WHAT IS CLAIMED IS:

1. A semiconductor memory sensing circuit in a memory array, comprising:

at lease one memory cell of a memory array, that generates a first voltage output and a second voltage output when the memory cell is accessed, wherein the first voltage output ramps from a predetermined voltage level to a higher voltage level, and the second voltage output keeps in a predetermined voltage level;

a first N-type device coupled between ground and one corresponding bit line of the memory array;

a second N-type device coupled between ground and one corresponding bit line-bar of the memory array; and

a differential amplifier with two input nodes coupled to the bit line and the bit line-bar of the memory array to generate a first sense output voltage if the first voltage output of one memory cell is higher than a second voltage output of the one memory cell and to generate a second sense output voltage if the first voltage output of one memory cell is lower than a second voltage output of the one memory cell.

2. The circuit as recited in claim 1, wherein the memory cell has at least one semiconductor device.

3. The circuit as recited in claim 1, wherein the memory cell has a static random access memory (SRAM) device.

4. The circuit as recited in claim 3, wherein the SRAM cell has at least one back-to-back inverting circuit with both inverting devices hooked up to VDD through a pull-up device and to Ground through a pull-down device.

5. The circuit as recited in claim 4, wherein the pull-up device has a P-type semiconductor device and the pull-down device has an N-type semiconductor device.

6. The circuit as recited in claim 4, wherein the pull-up device has a resistor and the pull-down device has another resistor.

7. The circuit as recited in claim 1, wherein the differential amplifier has an amplifier circuit with at least two differential input nodes and a control input for enabling and disabling the amplifier circuit.

8. A control circuit for a semiconductor memory array, comprising:

a sense amplifier for amplifying output from a memory cell; and

a self-timer coupled to the sense amplifier for counting a time and sending out control signals to shut off the sense amplifier according to the time and pulling down a word line to avoid further current sinking through the memory cell.

9. The circuit as recited in claim 8, further comprising

a delay device for controlling a second time to discharge a bit line and a bit line-bar of the memory array;

10. The circuit as recited in claim 8, wherein the self-timer counts the time of differentiating a voltage between the bit line and the bit line-bar.

11. The circuit as recited in claim 8, wherein when the differential voltage of the bit line and the bit line-bar reaches a predetermined threshold, the self-timer sends a signal to turn off the word line.

12. The circuit as recited in claim 8, wherein when the differential voltage of the bit line and the bit line-bar reaches a predetermined threshold, the self-timer sends a signal to enable the sense amplifier.

13. The circuit as recited in claim 9, wherein when the differential voltage of the bit line and the bit line-bar reaches a predetermined threshold, the delay device send a signal to discharge the bit line and bit line-bar.

14. The circuit as recited in claim 9, wherein the delay device postpones the time and sends a signal to turn on N-type devices to discharge the bit line and bit line-bar to avoid overlapping of the word line and the bit line and bit line-bar.